REMARKS

Claims 1-29, all the claims pending in the application, stand rejected on prior art grounds. Claims 1-10 stand rejected upon informalities. Claims 1, 5, 10, 11, 17, 21, and 26 are amended herein. Applicants respectfully traverse these rejections based on the following discussion.

I. The 35 U.S.C. §112, Second Paragraph, Rejection

Claims 1-10 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. These rejections are traversed as explained below. The Office Action suggests that "adjacent" does not have a clear meaning, and thus the Office Action presumes "adjacent" means near, but not touching. However, if the claims are properly read in conjunction with the specification and drawings, it is clear that adjacent means contacting. Nonetheless, in an effort to move forward with the prosecution, Applicants have amended claims 1, 5, 10, 11, 17, 21, and 26 to replace "adjacent to" with "contacting". Accordingly, the claims should be read in light of these changes. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

II. The Prior Art Rejections

Claims 1-9 stand rejected under 35 U.S.C. §102(e) as being anticipated by Fried et al. (U.S. Publication No. 2003/0178670), hereinafter referred to as "Fried". Claims 1-5, and 9-10 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lee et al. (U.S. Publication No. 2003/0042531), hereinafter referred to as "Lee". Claims 11-29 stand rejected under 35 U.S.C.

§102(e) as being anticipated by Mathew et al. (U.S. Publication No. 2005/0098822), hereinafter referred to as "Mathew". Applicants respectfully traverse these rejections based on the following discussion.

Fried teaches a device design and method for forming the same that result in Fin Field Effect Transistors having Non-Volatile Random Access Memory (NVRAM) capability. NVRAM capability arises from the presence of double floating gates arranged on and insulated from a semiconductor fin body, and a control gate arranged on and insulated from the double floating gates. The fabrication of the present device may be accomplished by providing an SOI wafer and defining a fin on the SOI wafer, the fin may be capped with an insulator layer; providing gate insulator on at least one vertical surface of the FIN; depositing floating gate material over the gate insulator; depositing insulator material on the floating gate material to form the floating gate isolation; depositing control gate material over the isolated floating gate material; removing a portion of the control gate material to expose source and drain regions of the Fin, implanting the Fin to form source/drain regions in the exposed regions of the Fin, and providing insulator material on the Fin. In addition, the NVRAM FinFET allows for horizontal current flow.

Lee teaches a flash memory element and its manufacturing method having improved overall memory characteristics by constituting a double-gate element for improving the scaling down characteristic of flash memory element. A flash memory element comprises a first oxide film formed on a surface of a silicon substrate; a fin active area vertically formed on the first oxide film; a gate tunneling oxide film formed on the fin active area; a floating electrode formed on the surfaces of the gate tunneling oxide film and the first oxide film; a inter-gates oxide film

formed on the surface of the floating electrode; and a control electrode formed on the surface of the inter-gates oxide film. With the above double-gate flash memory structure, a flash memory element in the present invention improves the scaling down characteristic and the programming and retention characteristic of a flash memory element.

Mathew teaches a transistor formed having three separately controllable gates. The three gate regions may be electrically biased differently and the gate regions may have different conductivity properties. The dielectrics on the channel sidewall may be different than the dielectrics on the top of the channel. Electrical contacts to the source and drain and the three gates is selectively made. By including charge storage layers, such as nanoclusters, adjacent the transistor channel and controlling the charge storage layers via the three gate regions, both volatile and non-volatile memory cells are realized using the same process to create a universal memory process. When implemented as a volatile cell, the height of the transistor and the characteristics of channel sidewall dielectrics control the memory retention characteristics. When implemented as a nonvolatile cell, the width of the transistor and the characteristics of the overlying channel dielectrics control the memory retention characteristics.

However, the claimed invention, as provided in amended independent claims 1, 11, and 21 contain features, which are patentably distinguishable from the prior art references of record. Specifically, claim 1 recites, in part, "...conducting spacers contacting said fin structure, wherein an upper surface of said conducting spacers is substantially planar with an upper surface of said fin structure; an insulator contacting said spacers, wherein said insulator is structurally isolated from said fin structure...." Additionally, claim 11 recites, in part, "...a third gate electrode positioned on top of said fin structure, said first gate electrode, and said second gate electrode."

Likewise, claim 21 recites, in part, "...depositing a third gate electrode on top of said fin structure, said first gate electrode, and said second gate electrode." These features are clearly provided in Applicants' FIGS. 3 through 12(b), as originally filed.

In Fried, the upper surface of the conducting spacers 115 is clearly non-planar with the upper surface of the fin structure 105 (see FIG. 11 in Fried) contrary to the Applicants' claimed invention. Moreover, in Fried, the insulator 110 is clearly not structurally isolated from the fin structure (see FIG. 11 in Fried) contrary to the Applicants' claimed invention. In fact, in the Applicants' claimed invention, and particularly in independent claim 1 (with reference to Applicants' FIGS. 3 through 12(b)), a FET 100 comprises a fin structure 170; conducting spacers 145 contacting said fin structure 170, wherein an upper surface of said conducting spacers 145 is planar with an upper surface of said fin structure 170; an insulator 155 adjacent to said spacers 145, wherein said insulator 155 is structurally isolated from said fin structure 170; and a gate layer 130 positioned on said fin structure 170, said spacers 145, and said insulator 155. Therefore, Applicants' claims 1-9 are patentably distinct from Fried.

In Lee, the Office Action characterizes the fin active area 26 as the fin structure. If such a characterization is proper, then the conducting spacers 38 are clearly not contacting to the fin structure 26 (see FIG. 5d of Lee) contrary to the Applicants' claimed invention. Additionally, in Lee the upper surface of the conducting spacers 38 is clearly non-planar with the upper surface of the fin structure 26 (see FIG. 5d of Lee) contrary to the Applicants' claimed invention. If the second oxide film 30 is considered part of the fin structure 26 in Lee, then the insulator 34 is clearly not structurally isolated from the fin structure (see FIG. 5d in Lee) contrary to the Applicants' claimed invention. In fact, in the Applicants' claimed invention, and particularly in

independent claim 1 (with reference to Applicants' FIGS. 3 through 12(b)), a FET 100 comprises a fin structure 170; conducting spacers 145 contacting said fin structure 170, wherein an upper surface of said conducting spacers 145 is planar with an upper surface of said fin structure 170; an insulator 155 adjacent to said spacers 145, wherein said insulator 155 is structurally isolated from said fin structure 170; and a gate layer 130 positioned on said fin structure 170, said spacers 145, and said insulator 155. Therefore, Applicants' claims 1-5, 9, and 10 are patentably distinct from Lee irrespective of how Lee is interpreted.

In Mathew (see FIGS. 4 and 5), the gate electrode 18 is clearly not contacting the fin structure 14 as the gate insulator 16 separates the gate electrode 18 from the fin structure 14. Even if gates 42 or 44 in Mathew are considered to be the "first gate electrode", then neither of these gates contacts the fin structure 14 as oxide layer 26 separates each of the gates 42, 44 from the fin structure 14, contrary to the Applicants' claimed invention. Additionally, in Mathew (see FIGS. 4 and 5) the gate electrode 42 is clearly not positioned on top of the fin structure 14, gate electrode 18, and the gate electrode 44, contrary to the Applicants' claimed invention. If Mathew is interpreted such that gate electrode 18 is the "third gate electrode", then gates 42 and 44 are the second and third gate electrodes (or vice versa). In such an interpretation, while gate electrode 18 is positioned on top of the fin structure 14, it is not, however, positioned on top of the gate electrodes 42, 44 (as shown in FIG. 5 of Mathew, there is no structure on top of gates 42, 44). In fact, in the Applicants' claimed invention, and particularly in independent claim 11 (with reference to Applicants' FIGS. 3 through 12(b)), a FET device 100 comprises a fin structure 170; a first gate electrode 145 adjacent to said fin structure 170; a gate insulator 160 positioned between said first gate electrode 145 and said fin structure 170; a second gate

electrode 140 positioned transverse to said first gate electrode 145; and a third gate electrode 130 positioned on top of said fin structure 170, said first gate electrode 145, and said second gate electrode 140. Furthermore, in the Applicants' claimed invention, and particularly in independent claim 21 (with reference to Applicants' FIGS. 3 through 13), a method of lowering a gate capacitance and extrinsic resistance in a FET 100 comprises forming (205) a fin structure 170; configuring (207) a first gate electrode 145 contacting said fin structure 170; disposing (209) a gate insulator 160 between said first gate electrode 145 and said fin structure 170; positioning (211) a second gate electrode 140 transverse to said first gate electrode 145; and depositing (213) a third gate electrode 130 on top of said fin structure 170, said first gate electrode 145, and said second gate electrode 140. Therefore, Applicants' claims 11-29 are patentably distinct from Mathew irrespective of how Mathew is interpreted.

Moreover, the Applicants note that all claims are properly supported in the specification and accompanying drawings. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

III. Formal Matters and Conclusion

With respect to the rejections to the claims, the claims have been amended, above, to overcome these rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

In view of the foregoing, Applicants submit that claims 1-29, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to

issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

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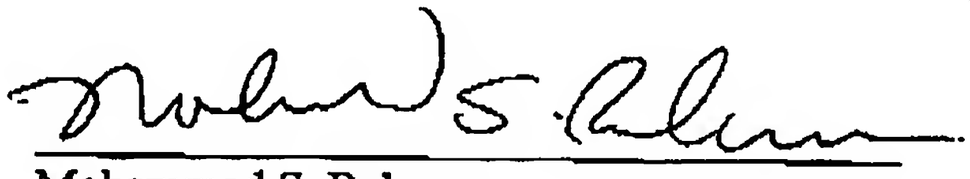

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